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T. Kohonen, Content-Addressable Memories, 2nd ed., Springer-Verlag, Berlin, 1987.  
S. D. Kuth, The Art of Computer Programming, Sorting and Searching, ...  
doi:leecocomputersociety.org/10.1109/40.141803 - Similar pages

psu Content-Addressable and Associative Memory

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Common bit arrangement for content-addressable memory... T. Kohonen.  
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doi:leecocomputersociety.org/10.1109/2.30732 - Similar pages

eBay - Book: Content Addressable Memories (ISBN: 0387098232)

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T. Kohonen, Content-Addressable Memories, Springer Series in Information Sciences, vol. 1, Springer Berlin Heidelberg 1987 ...  
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Content-Addressable and Associative Memory

H. Kadoa et al., An 8-bit Content-Addressable and Reentrant Memory, ... 8 T. Kohonen, Content-Addressable Memories, Springer-Verlag New York, Inc., ...  
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psu A Hardware Implementation of Gridless Routing Based on Content...

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50-53. rasnussen, rd ; boblin, ge ; dinopoulos, nj ; lewis, ef ; manning, ...  
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Associative Processor" year: 1989 Journal: ...  
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ICPP 1987  
International Conference on Parallel Processing (ICPP 87). University Park, PA,  
USA, August 1987. Pennsylvania State Univ. Press, 1987 ...  
[sunsite.online.globeule.org/dbip/db/indices/a-tree/ligen/Senior.html](http://sunsite.online.globeule.org/dbip/db/indices/a-tree/ligen/Senior.html) - 64k - Supplemental Result - Cached - Similar pages

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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

☐ 1. An asynchronous distributed approach for the simulation of behavior-level parallel processors

Ghosh, S.; Meng-Lin Yu;

Parallel and Distributed Systems, IEEE Transactions on

Volume 6, Issue 6, June 1995 Page(s):639 - 652

Digital Object Identifier 10.1109/71.388044

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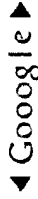
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Dalton., Neosera Systems Ltd, NovaUCD, Belfield, Dublin 4, Ireland. ...

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## Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

☐ 1. Parallel logic simulation on a network of workstations using PVM

Kornicki, M.; Mahmood, A.; Carlson, B.S.;

Parallel and Distributed Processing, 1996. Eighth IEEE Symposium on

23-26 Oct. 1996 Page(s):2 - 9

Digital Object Identifier 10.1109/SPDP.1996.570310

AbstractPlus | Full Text: PDF(728 KB) IEEE CNF

☐ 2. Parallel event-driven logic simulation algorithms: tutorial and comparative

Baker, W.I.; Mahmood, A.; Carlson, B.S.;

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G

and Systems]

Volume 143, Issue 4, Aug. 1996 Page(s):177 - 185

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☐ 3. Study of a multilevel approach to partitioning for parallel logic simulation

Subramanian, S.; Rao, D.M.; Wiley, P.A.;

Parallel and Distributed Processing Symposium, 2000. IPDPS 2000. Proceedin

International

1-5 May 2000 Page(s):833 - 838

Digital Object Identifier 10.1109/IPDPS.2000.846071

AbstractPlus | Full Text: PDF(172 KB) IEEE CNF

☐ 4. Parallel-and-vector implementation of the event-driven logic simulation a

Cray Y-MP supercomputer

Batalineh, A.; Ozguner, F.;

Supercomputing '92. Proceedings

16-20 Nov. 1992 Page(s):444 - 452

Digital Object Identifier 10.1109/SUPERC.1992.236659

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☐ 5. Logic simulation using an asynchronous parallel discrete-event simulatio

SMD machine

Seth, S.; Gowen, L.; Payne, M.; Sylvester, D.;

VLSI Design, 1994., Proceedings of the Seventh International Conference on

5-8 Jan. 1994 Page(s):29 - 32

Digital Object Identifier 10.1109/ICVD.1994.282635

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☐ 6. Cone clustering principles for parallel logic simulation

Heiting, K.; Rallein, R.; Trautmann, S.;

Modeling, Analysis and Simulation of Computer and Telecommunications Syst

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11-16 Oct. 2002 Page(s):93 - 100

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☐ 7. Modular construction of model partitioning processes for parallel logic si

Heiting, K.; Rungger, G.; Trautmann, S.;

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Digital Object Identifier 10.1109/CPWP.2001.951858

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☐ 8. Distributed logic simulation algorithm using preemption of inconsistent e

Raghu, C.S.; Sundaram, S.;

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4-7 Jan. 1998 Page(s):482 - 487

Digital Object Identifier 10.1109/ICVD.1998.646653

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☐ 9. Distributed logic simulation: time-first evaluation vs. event driven algorit

Sundaram, S.; Patnaik, L.M.;

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☐ 10. Accelerated logic simulation using parallel processing

Hoppe, P.;

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11-14 April 1998 Page(s):156 - 163

Digital Object Identifier 10.1109/CMPEUR.1998.4948

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☐ 11. Parallel logic simulation using Time Warp on shared-memory multiproce

Kim, H.K.; Chung, S.M.;

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26-29 April 1994 Page(s):942 - 948

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☐ 12. An analysis of parallel synchronous and conservative asynchronous log

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- ☐ 15. Parallel logic simulation on general purpose machines  
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- ☐ 16. Efficient parallel logic simulation techniques for the Connection Machine  
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- ☐ 17. High speed VLSI logic simulation using bitwise operations and parallel p  
Jun, Y.-H.; Hajj, I.N.; Lee, S.-H.; Park, S.-B.;  
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- ☐ 19. A parallel algorithm for logic simulation on transputer networks  
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- ☐ 20. Time warp for efficient parallel logic simulation on a massively parallel S  
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- ☐ 21. Comparisons and analysis of massively parallel SIMD architectures for p  
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- ☐ 23. Parallel Logic Simulation of Million-Gate VLSI Circuits  
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